REMARKS

Claims 1-21 are pending in the application.

Claims 1 and 7-21 are allowed.

Claims 2-6 are objected to.

Claim 2 is amended.

No new matter is added.

Claims 1-21 remain in the case.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Allowable Subject Matter

Applicant thanks the Examiner for indicating that claims 1 and 7-21 are allowed.

Drawings

The Examiner has stated that Figure 1 should be designated by a legend such as --Prior Art—because only that which is old is illustrated.

Applicant submits herewith sketches showing proposed addition of the legend --Prior Art-- to drawing FIG. 1 with changes highlighted in accordance with MPEP 608.02(v). Applicant requests the Examiner's approval of the proposed changes in accordance with 37 CFR 1.121 and MPEP 608.02(q).

Specification

The Examiner has stated that the title of the invention is not descriptive. The title is amended to read "Method of forming a non-volatile memory device having floating trap type memory cell," which is clearly indicative of the invention to which the claims are directed, as suggested by the Examiner.

Claim Objections

The Examiner has objected to Claims 2-6 because of the following informalities:

Re claim 2, the phrase "(g) removing the second conductive layer and the triple layer of the respective high-and low-voltage type gate patterns" is misdescriptive because the high- and low-voltage type gate patterns do not have the second conductive layer and the triple layer. The second conductive layer and the triple layer are formed only on the exposed

substrate in the cell array region (see step e). Claims 3-6 are objected because each includes the limitations of independent claim 2.

Claim 2 is amended to recite,

"d) removing a portion of the first conductive layer in the cell array region to expose a region of the substrate;

(e) sequentially forming a triple layer and a second conductive layer on the resulting structure including the first conductive layer and the exposed region of the substrate, the triple layer including a tunneling insulating layer, a charge storage layer, and a blocking insulating layer;

(f) patterning a substrate where the second conductive layer is formed, whereby forming a cell gate pattern in the cell array region and forming high-and low-voltage-type gate patterns in the peripheral high-and low-voltage regions, respectively;

(g) removing a portion of the second conductive layer and a portion of the triple layer of the respective high-and low-voltage-type gate patterns to form a butting region exposing the first polysilicon layer;

(h) forming and patterning an interlayer insulating layer over substantially the entire surface of the substrate to form contact holes including a butting contact hole extending over the butting region; and

(i) forming a contact plug to fill the contact holes."

Therefore, the phrase (e) was corrected to state that sequentially forming a triple layer and a second conductive layer on the resulting structure including the first conductive layer and the exposed region of the substrate. Please note that "in the cell array region" is omitted to make it clear that the triple layer and the second conductive layer is formed not only on the exposed substrate in the cell array region, but on other non-cell array regions.

The amendments are supported in the specification, for example, at page 7, line 8-page 8, line 11; and FIGS. 2-7. Particularly please see FIG. 5 and the accompanying text.

Now with the proper description of the claimed invention, one skilled in the art will appreciate what is meant by "removing a portion of the second conductive layer and a portion of the triple layer of the respective high-and low-voltage-type gate patterns to form a butting region exposing the first polysilicon layer," as recited in claim 2, for example, in view of FIG. 5 of the present application.

Thus, the objection to the claim 2 and claims 3-6, which depend therefrom, are now overcome.

For the foregoing reasons, reconsideration and allowance of claims 1-21 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

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Limited Recognition Under 37 CFR § 10.9(b)

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date: October 15, 2004

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Angie C, Farr

IN THE DRAWINGS

Applicant submits herewith sketches showing proposed addition of the legend --Prior Art-- to drawing FIG. 1 with changes highlighted in accordance with MPEP 608.02(v). Applicant requests the Examiner's approval of the proposed changes in accordance with 37 CFR 1.121 and MPEP 608.02(q).

Annotated Sheet Showing Changes

Fig. 1 (Prior Art)